

WHAT IS CLAIMED IS:

- Sub  
Q4
1. A circuit package, comprising:  
a dielectric substrate having a first surface and a second surface, disposed opposite to said first surface, and a via extending therebetween, with a first conductor disposed on said surface and extending from said via, and a second conductor disposed on said second surface and extending from said via, with said via placing said first and second conductors in electrical communication; and  
a driver circuit mounted to said substrate and including an input and an output, with said output being in electrical communication with said first conductor and having an output resistive component associated therewith, with said via having a resistive fill disposed therein, defining a via resistance connected between said first and second conductors, said output having an output impedance being defined by said output resistive component and said via resistance.
2. The circuit as recited in claim 1 wherein said via resistance has a value associated therewith to be a dominant component of said output impedance.
3. The circuit package as recited in claim 1 wherein said substrate further includes an additional conductor and an additional via filled with said resistive fill, defining an additional via resistance, said additional conductor being disposed on said first side and extending from said additional via, with said second conductor being in electrical communication with

FOUOCT 11 1990

said additional via with said additional via resistance extending between said additional and second conductors and said input being in electrical communication with said additional conductor and having an input resistance component and an input impedance associated therewith, with said input impedance being defined by said input resistive component and said additional via resistance.

4. The circuit package as recited in claim 1 wherein said substrate includes a plurality of said via, a subgroup of which extends between said first and second conductors in parallel and have said resistive fill disposed therein to define said resistance, with said resistance being inversely proportional to a number of said plurality of vias in said subgroup.

5. The circuit package as recited in claim 1 wherein said via resistance has a magnitude that is at least twice a magnitude of said output resistive component.

6. The circuit package as recited in claim 1 wherein said output resistive component further includes an output resistance of said driver circuit having a magnitude in a range of 5 to 12 ohms, inclusive, with said resistance having a magnitude in a range of 35 to 50 ohms, inclusive.

7. The circuit package as recited in claim 1 wherein said substrate is a printed circuit board.

8. The circuit package as recited in claim 1 wherein said driving circuit is selected from a set of

Chf  
Su  
Q4

100224-122001

driving circuits consisting of, a buffer, as inverter and an amplifier.

9. A circuit, comprising:

a dielectric substrate having a first surface and a second surface, disposed opposite to said first surface and a plurality of vias extending therebetween, with first and second conductors disposed on said first surface and a third conductor disposed on said second surface, with said first and third conductors and extending from a first of said plurality of vias and said second and third conductors extending from a second of said plurality of vias;

a driver circuit mounted to said substrate and including an output having an output resistive component associated therewith, and an input having an input resistive component associated therewith, with said output being in electrical communication with said first conductor and said input being in electrical communication with said second conductor, with said first via having a resistive fill disposed therein defining a first via resistance connected between said first and third conductors and said second via having said resistive fill disposed therein defining a second via resistance connected between said second and third conductors said output having an output impedance associated therewith defined by said output resistive component and said first via resistance first via resistance, having a magnitude that is at least twice a magnitude of said output resistive component, with said input having an input impedance associated therewith defined by said input resistive component and said second via resistance, with said second via resistance having a

CONFIDENTIAL

magnitude that is at least twice a magnitude of said input resistive component.

10. The circuit package as recited in claim 9 wherein a first subgroup of said plurality of said vias extends between said first and third conductors in parallel and have said resistive fill disposed therein to define said first resistance, with said first resistance being inversely proportional to a number of said plurality of vias in said first subgroup.

11. The circuit package as recited in claim 10 wherein a second subgroup of said plurality of said vias extends between said second and third conductors in parallel and have said resistive fill disposed therein to define said second resistance, with said second resistance being inversely proportional to a number of said plurality of vias in said first subgroup.

12. The circuit package as recited in claim 11 wherein said input and output resistances of said driver circuit each have a magnitude in a range of 5 to 12 ohms, inclusive, with said first and second resistances having a magnitude in a range of 35 to 50 ohms, inclusive.

13. The circuit package as recited in claim 12 wherein said substrate is a printed circuit board.

14. The circuit package as recited in claim 13 wherein said driving circuit is selected from a set of driving circuits consisting of, a buffer, an inverter and an amplifier.

Cont  
Sub  
A4

10028814-122001

15. A method of establishing an impedance of a circuit package, said method comprising:

attaching said circuit driver to a dielectric substrate having a first surface and a second surface, disposed opposite to said first surface and a via extending therebetween, with a first conductor disposed on said surface and extending from said via and a second conductor disposed on said second surface and extending from said via, with said via placing said first and second conductors in electrical communication, with said driver circuit including an input and an output, with said output being in electrical communication with said first conductor and having an output impedance associated therewith that includes an output resistive component and an output reactance component; and

filling said via with a resistive fill to define a resistance connected between said first and second conductors, with said resistance being of sufficient magnitude to define dominant component of said output impedance.

16. The method as recited in claim 15 further including connecting said input to an additional conductor disposed on said first side of said substrate that is connected to an additional via, with said additional via extending from said additional conductor to said second conductor and filling said additional via with said resistive fill to define an additional resistance connected between said additional and second conductors with input resistive component including said additional resistance and being a dominant component of said input impedance.

Cont  
Sub  
Ay  
FOOZET-788200T

17. The method as recited in claim 15 further including adjusting said output resistance by connecting additional via between said first and second conductors and filling said additional via with said resistive fill to create a plurality of resistive vias connected in parallel between said first and second conductors, with said first resistance being inversely proportional to a number of said plurality of said resistive vias.

18. The method as recited in claim 17 further including adjusting said input resistance by connecting an additional via between said additional and second conductors and filling said additional via with said resistive fill to create a plurality of resistive vias connected in parallel between said additional and second conductors, with said additional resistance being inversely proportional to a number of said plurality of said resistive vias.

19. The method as recited in claim 15 wherein attaching said circuit driver further includes connecting said output to said first conductor at a region positioned spaced-apart from said via, with a length of said first conductor extending between said via and said region defining an interval having a resistance associated therewith, defining an interval resistance, with said output resistive component further including an output resistance of said driver circuit and said interval resistance, with said resistance having a magnitude at least twice a magnitude of said output resistance and said interval resistance, combined.

Comp  
Sub  
Ref

10028814-12004

20. The method as recited in claim 16 wherein attaching said circuit further includes connecting said input to said additional conductor at a region positioned spaced-apart from said additional via, with a length of said additional conductor extending between said additional via and said region defining an interval having a resistance associated therewith, defining an interval resistance, with said input resistive component further including an input resistance of said driver circuit and said interval resistance, with said additional resistance having a magnitude at least twice a magnitude of said input resistance and said interval resistance, combined.

Cont  
Sub  
A4

1002881-12001